LISTING OF THE CLAIMS

A detailed listing of claims is presented below. Please amend currently amended claims as indicated below including substituting clean versions for pending claims with the same number. In addition, clean text versions of pending claims not being currently amended that are under examination are also presented. It is understood that any claim presented in a clean version below has not been changed relative to the immediate prior version.

1. Cancelled in Transmittal.

2. Cancelled in Transmittal.

3. Cancelled in Transmittal.

4. Cancelled in Transmittal.

5. Cancelled in Transmittal.

6. Previously canceled.

7. Cancelled in Transmittal.

8. Cancelled in Transmittal.

9. Cancelled in Transmittal.

10. Cancelled in Transmittal.

11. Cancelled in Transmittal.

12. Cancelled in Transmittal.

13. Cancelled in Transmittal.

14. Previously canceled.

15. Cancelled in Transmittal.

16. Cancelled in Transmittal.

17. Cancelled in Transmittal.

18. Cancelled in Transmittal.

19. Cancelled in Transmittal.

20. Cancelled in Transmittal.

21. Cancelled in Transmittal.

22. Previously canceled.

23. Cancelled in Transmittal.

24. Cancelled in Transmittal.

25. Cancelled in Transmittal.

26. Cancelled in Transmittal.

27. Cancelled in Transmittal.

28. Cancelled in Transmittal.

29. Cancelled in Transmittal.

30. Previously canceled.

31. Cancelled in Transmittal.

32. Cancelled in Transmittal.

33. Cancelled in Transmittal

34. (Original) A vernier alignment structure for measuring distance comprising:

a transmitter chip comprising a plurality of transmitter pads spaced along a first line at a pitch of x, said transmitter chip

actively driving complementary waveforms from an input signal in an alternating pattern over said plurality of transmitter pads;

a receiving chip comprising a plurality of receiving pads spaced along a second line at a pitch of y, said first line in parallel with said second line and separated by a distance; and

a plurality of sensing circuits coupled to said plurality of receiving pads, said plurality of sensing circuits able to measure a change in said distance through capacitive coupling between said plurality of transmitting pads and said plurality of receiving pads.

35. (Original) The vernier alignment structure as described in Claim 34, wherein at least one of said plurality of sensing circuits comprises:

a CMOS inverter amplifier coupled to an input node, said CMOS inverter amplifier for amplifying a second input signal from an associated receiving pad;

a resistive feedback circuit coupled to said CMOS inverter amplifier and for cancelling an offset voltage associated with said CMOS inverter amplifier;

a bias circuit coupled to said resistive feedback circuit and for biasing said resistive feedback circuit in a minimally on state to maintain high impedance for said resistive feedback circuit; and

a clamping circuit coupled to said resistive feedback circuit for restricting output swing of an output signal of said CMOS inverter amplifier to maintain said high impedance.

36. (Original) The vernier alignment structure as described in Claim 34, wherein said plurality of sensing circuit are able to measure said distance.

37. (Original) The vernier alignment structure as described in Claim 34, wherein said input signal is a clock signal.

38. (New) The vernier alignment structure as described in Claim 34, further comprising:

an inverter coupled to said input signal for providing said complementary clock waveforms.

39. (New) The vernier alignment structure as described in Claim 34, wherein said plurality of receiving pads number less than said plurality of transmitter pads.

40. (New) The vernier alignment structure as described in Claim 34, wherein each of said plurality of receiving pads have approximately 10fF of parasitic capacitance.

41. (New) The vernier alignment structure as described in Claim 35, wherein said second input signal comprises a capacitively coupled differential clock signal from said plurality of transmitting pads and said plurality of receiving pads.

42. (New) The vernier alignment structure as described in Claim 41, wherein said differential clock signal comprises a 3.3 volt clock signal coupled through a minimum of 0.1fF differential coupling capacitance and having a frequency of between 0-20 MHz.

43. The vernier alignment structure as described in Claim 35, wherein said resistive feedback circuit biases said CMOS inverter amplifier to a threshold voltage associated with said CMOS inverter amplifier to cancel said offset voltage.

44. The vernier alignment structure as described in Claim 35, wherein said resistive feedback circuit comprises:

a PMOS transistor comprising a PMOS source coupled to an output of said CMOS inverter amplifier that provides said output signal, a PMOS gate, and a PMOS drain coupled to said input node; and

an NMOS transistor comprising an NMOS drain coupled to said PMOS source, an NMOS gate, and an NMOS source coupled to said output.

45. The vernier alignment structure as described in Claim 35, wherein said bias circuit comprises:

a second CMOS inverter amplifier of similar dimension to said CMOS inverter amplifier, said second CMOS inverter amplifier comprising a PMOS transistor and an NMOS transistor in a standard inverter configuration; and

an NMOS diode coupled in series between said PMOS transistor and said NMOS transistor, said NMOS diode for providing a p-bias voltage from said PMOS transistor to said resistive feedback circuit that is slightly lower than a threshold voltage associated with said CMOS inverter amplifier, and an n-bias voltage from said NMOS transistor that is slightly higher than said threshold voltage.

46. The vernier alignment structure as described in Claim 35, wherein said clamp circuit comprises:

a PMOS transistor comprising a PMOS source coupled to an output of said CMOS inverter amplifier that provides said output signal, a PMOS gate coupled to a first bias voltage slightly lower than a threshold voltage of said CMOS inverter amplifier, and a PMOS drain coupled to a bias node;

said bias node;

an NMOS transistor comprising an NMOS drain coupled to bias node, an NMOS gate coupled to a second bias voltage slightly higher than said threshold voltage, and an NMOS source coupled to said output; and

a second CMOS inverter amplifier of similar dimension to said CMOS inverter amplifier, and comprising a second input coupled to said bias node and a second output coupled to said bias node.

47. The vernier alignment structure as described in Claim 35, wherein said CMOS inverter amplifier is a first amplification stage, and further comprising:

a second amplification stage comprising a second CMOS inverter amplifier coupled to said output, said second CMOS inverter amplifier of similar dimension and configuration as said CMOS inverter amplifier; and

a third amplification stage comprising a third CMOS inverter amplifier coupled to said second CMOS inverter amplifier.